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# Processor Architecture

From Dataflow to Superscalar and Beyond



Springer

# Procebor Architecture From Dataflow To Superscalar And Beyond

**Desző Sima, Péter Kacsuk**



## **Procebor Architecture From Dataflow To Superscalar And Beyond:**

*Processor Architecture* Jurij Silc, Borut Robic, Theo Ungerer, 1999-06-08 A survey of architectural mechanisms and implementation techniques for exploiting fine and coarse grained parallelism within microprocessors Beginning with a review of past techniques the monograph provides a comprehensive account of state of the art techniques used in microprocessors covering both the concepts involved and implementations in sample processors The whole is rounded off with a thorough review of the research techniques that will lead to future microprocessors XXXXXXXX Neuer Text This monograph surveys architectural mechanisms and implementation techniques for exploiting fine grained and coarse grained parallelism within microprocessors It presents a comprehensive account of state of the art techniques used in microprocessors that covers both the concepts involved and possible implementations The authors also provide application oriented methods and a thorough review of the research techniques that will lead to the development of future processors **Advanced Topics in Dataflow**

**Computing and Multithreading** Guang R. Gao, Lubomir Bic, Jean-Luc Gaudiot, 1995-07-14 The book includes papers on massively parallel distributed memory and multithreaded architecture design synchronization and pipelined design and superpipelined data driven VLSI processors Other sections discuss stream data types the development of well structured software and parallelization of dataflow programs **A dataflow/von Neumann hybrid architecture** Robert A. Iannucci, 1988 This report examines the spectrum of architectures from von Neumann to dataflow by proposing a new architecture which is a hybrid of the two paradigms The analysis attempts to discover those features of the dataflow architecture lacking in a von Neumann machine which are essential for tolerating latency and synchronization costs These features are captured in the concept of a parallel machine language wherein the units of scheduling called scheduling quanta are bound at compile time rather than at instruction set design time It is shown that the combination of dataflow style explicit synchronization and von Neumann style implicit synchronization results in an architectural synergism Using an instruction set which is strictly less powerful than that of the MIT Tagged Token Dataflow TTDA the hybrid architecture can exploit the same kinds of parallelism while executing fewer instructions demonstrating the power of passing state implicitly between program counter sequenced instructions Keywords Multiprocessors KR *Selected Reprints on Dataflow and Reduction Architectures* S. S. Thakkar, 1987 **Associative Dataflow Processor Architecture** Tariq Jamil, 1996

**Advanced Computer Architectures** Desz? Sima, P?ter Kacsuk, 1997 This timely book provides an unconventional and up to date overview of all the important computer architectures and is one of the first texts to present all the relevant concepts of advanced architecture classes by exploring their design spaces Advanced Computer Architectures will prove an indispensable guide for anyone who needs to be acquainted with the relevant concepts and solutions introduced in recent years to the dramatically changing world of computer architecture For the student of advanced level courses in computer architecture this book will provide a comprehensive and accessible overview of the subject whilst its strong practical

orientation will make it an invaluable reference for the practitioner Features Explores design spaces for each architecture class and exposes evolution of concepts and design issues Provides an up to date overview of significant architecture classes including unique in depth coverage of superscalar architectures as well as multithreaded shared and distributed memory MIMDs and associative and neural architectures Identifies which concepts and design choices have been made use of in important processors and illustrates significant trends and surpassed and viable concepts Case studies and tables show microarchitectural details of relevant processors including the PentiumPro PowerPC 604 PowerPC 620 and R10000 allowing comparisons between them 0201422913B04062001 *The Microarchitecture of Pipelined and Superscalar Computers* Amos R. Omondi,1999-04-30 This book is intended to serve as a textbook for a second course in the implementation Le microarchitecture of computer architectures The subject matter covered is the collection of techniques that are used to achieve the highest performance in single processor machines these techniques center the exploitation of low level parallelism temporal and spatial in the processing of machine instructions The target audience consists students in the final year of an undergraduate program or in the first year of a postgraduate program in computer science computer engineering or electrical engineering professional computer designers will also also find the book useful as an introduction to the topics covered Typically the author has used the material presented here as the basis of a full semester undergraduate course or a half semester post graduate course with the other half of the latter devoted to multiple processor machines The background assumed of the reader is a good first course in computer architecture and implementation to the level in say Computer Organization and Design by D Patterson and H Hennessy and familiarity with digital logic design The book consists of eight chapters The first chapter is an introduction to all of the main ideas that the following chapters cover in detail the topics covered are the main forms of pipelining used in high performance uniprocessors a taxonomy of the space of pipelined processors and performance issues It is also intended that this chapter should be readable as a brief stand alone survey **A**

**Dataflow Architecture with Improved Asymptotic Performance** Robert E. Thomas,1981 *The Super-actor Machine*  
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