

Design of a 32-b Monolithic Microprocessor Based on GaAs HEMSFET Technology

Chien-Kuo V. Tien, Kelvin Lewis, Hans J. Grieb, Tom Tsien, and John F. McDonald

Abstract—This paper examines the design of a 32-b GaAs Fast RISC microprocessor (F-RISC/O). F-RISC/O is a single chip GaAs HEMSFET processor targeted for implementation on a multichip module (MCM) together with cache memories. The CPU architecture, circuit design, implementation, and testing are optimized for a seven-stage instruction pipeline implemented with GaAs super-buffered FET logic (SBFL). We have been able to verify novel GaAs SBFL standard cells and compare measured CPU performance with performance estimates based on circuit and device models. The prototype 32-b microprocessor has been implemented using an automated standard cell approach because of time constraints and fabricated using an experimental process by Rockwell International. The CPU chip integrates 92,348 transistors on a 7×7 mm² die and dissipates 6.13 W at 180 MHz. Test results from a prototype fabrication run have demonstrated the operation of the ALU, the program counter, and the register file with delays below 6, 5, and 2.4 ns, respectively. The successful modeling and verification indicate that a 6.5 μ m HEMSFET implementation of F-RISC/O could achieve a peak performance of 350 MHz. The wiring delays account for 42% of the critical path delay.

Index Terms—GaAs HEMSFET, instruction pipeline, microprocessor design, multichip module (MCM), reduced instruction set computer (RISC), super-buffered FET logic (SBFL).

I. INTRODUCTION

Recent advances in GaAs Heterojunction MESFET (HEMSFET) technology have led to gate delays below 100 ps [1] and higher integration levels, reaching VLSI complexity and, thereby, allowing the implementation of a 32-b GaAs RISC on a single chip [2]. However, integration levels are still very low compared to CMOS and do not allow the inclusion of sufficiently large caches on the chip. The cache memories must be implemented with high speed SRAM chips which need to be placed close to the CPU chip on an MCM to keep the interconnect delays low. The processor design, therefore, must consider the interactions between architecture, circuit technology, and MCM packaging. The main issues in GaAs microprocessor design are the processor versus memory speed mismatch and the limited off-chip communication bandwidth.

To overcome the difficulties of limited yield and low I/O bandwidth in GaAs, the high speed processing mode, consisting of the processor and cache memory hierarchy, must be densely implemented on an MCM [3], [4]. F-RISC/O employs further a pipelined cache memory access [5] to "hide" some of the chip-to-chip delays in pipeline stages since, even on an MCM, the address and data transfer times between chips are of the same order as the processor delays.

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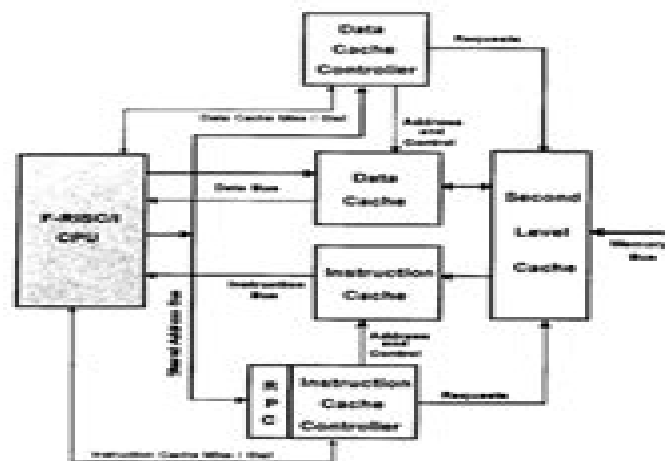


Fig. 1. F-RISC/O MCM system.

The primary goals of the Fast RISC/O (F-RISC/O) project were to verify the novel GaAs SBFL standard cells, to verify that HEMSFET yields have reached adequate levels, and to correlate measured CPU performance with simulations based on circuit and device models to check the modeling capabilities of our CAD tools. F-RISC/O is a companion project to the ARPA sponsored heterojunction bipolar transistor (HBT) F-RISC project.

II. GAAS MICROPROCESSOR DESIGN

Fig. 1 shows the F-RISC/O MCM system. High memory bandwidth is achieved using separate instruction and data caches with their own data buses. This allows one 32-b instruction and one 32-b data word to be supplied by the cache memories in each cycle. A shared address bus is used to communicate with both the instruction and data cache memories to reduce CPU pin count and interconnections. This requires a remote program counter (RPC) on the instruction cache controller. Using the RPC the instruction cache can access consecutive instructions without an address transfer from the CPU. The instruction memory needs an address from the CPU only if a branch or an exception is taken. The shared address bus never causes contention in this scalar architecture since load/store and branch instructions are designed to use the address bus in the same pipeline stage.

The relative performance figure of a processor implementation is usually expressed in MIPS (millions of instructions per second), and is inversely proportional to the cycle time T_{CPI} and the average number of Cycles per Instruction (CPI). The principal parameters affecting T_{CPI} are the GaAs circuit technology and the pipeline. The CPI for a scalar RISC processor is basically one instruction cycle plus the average number of wasted cycles due to pipeline hazards, such as branch and load penalties, and stall cycles after cache misses. The CPU/system performance must be optimized by considering both the architecture (especially the pipeline scheme) and

Microprocessor Design For Gaas Technology

Bruce Allen Bernhardt



Microprocessor Design For GaAs Technology:

Microprocessor-design for GaAs Technology Veljko Milutinović, Purdue University. School of Electrical Engineering, 1986

Microprocessor Design for GaAs Technology Veljko Milutinović, 1990

Foundations of Computer Technology Alexander John Anderson, 2020-10-25

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Tutorial--gallium Arsenide Computer Design Veljko Milutinović, David A. Fura, 1988

Supercollider 2 Michael McAshan, 2012-12-06

The Second International Industrialization Symposium on the Supercollider IISCC was held in Miami Beach Florida on March 14 16 1990 It was an even bigger and more successful meeting than our first in New Orleans in 1989 There were 691 attendees and 75 exhibitors The enthusiasm shown by both the speakers and the audience was exhilarating for all attendees The symposium again brought together the physicists and engineers designing the machine the industrial organizations supporting the design and construction the education community and the governmental groups responsible for the funding and management of the SSC project We believe it is this unique mix which makes this particular meeting so valuable The theme of this symposium was The SSC Americas Research Partnership and the varied presentations throughout the meeting highlighted that theme The keynote speakers were Dr Roy Schwitters Director of the SSC Mr Paul F Orefitce Chairman of the Board of Dow Chemical Company Honorable W Hinson Moore Deputy Secretary of Energy Mr Morton Meyerson Chairman of the Texas National Research Laboratory Commission Honorable Robert A Roe Congressman from New Jersey and Chairman House Science and Technology Committee Honorable Tom Bevel Representative from Alabama Chairman House Energy and Water Development Appropriation Subcommittee In addition there was a discussion of issues by a panel of four Congressmen Honorable Jim

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Advanced Microprocessors, II Amar Gupta,1987 **Surviving the Design of a 200 MHz RISC Microprocessor** Veljko Milutinović,1997 Learn all the intricacies of the design of a 32 bit RISC microprocessor developed through the first DARPA effort to create a 200 MHz processor on a VLSI chip This book takes you through all phases of this project and covers all the theoretical and technical details necessary for the creation of the final architecture and design It places special emphasis on the research and development methodology utilized in the project The methodology described in this book includes the following elements creation of a candidate architecture comparative testing on the functional level selection and final refinement of the best architecture transformation from the architecture level to the design level logical and timing testing of the design and presentation for fabrication The text details how software tools are used in this project and how RISC architecture serves as the baseline for the project It covers specific design techniques languages testing phases architectural issues implementation technology and applications The book tested in a number of university courses and commercial tutorials is ideal for various undergraduate courses devoted to microprocessor design for VLSI International Journal of Mini & Microcomputers ,1995 Gallium Arsenide Technology David K. Ferry,1985 DARPA Technical Accomplishments Sidney G. Reed,1991 **Proceedings, IEEE International Conference on Computer Design, VLSI in Computers** ,1985 1995 4th International Conference on Solid-State and Integrated Circuit Technology International Conference on Solid-State and Integrated Circuit Technology,IEEE Electron Devices Society,1995 Gallium Arsenide Technology ,1985 **Microcomputers--usage, Methods, and Structures** Harald Schumny,John Mølgaard,1987 Accurate Timing Simulation of Digital Gallium Arsenide Circuits Bruce Allen Bernhardt,1990 **Scientific and Technical Aerospace Reports** ,1994 1991 IEEE International Symposium on Circuits and Systems ,1991 Annual Connectors and Interconnection Technology Symposium Proceedings ,1989 GaAs Integrated Circuits Joseph Mun,1988

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