

## VLSI Implementations of a Reduced Instruction Set Computer

Daniel T. Fitzpatrick, Manolis G.H. Katevenis, David A. Patterson, Zvi Peshkess, Robert W. Sherburne, John K. Foderaro, Howard A. Landman, James B. Peek, Carlo H. Séquin, and Korbin S. Van Dyke

University of California at Berkeley  
Computer Science Division/EECS Department  
Berkeley, California 94720

### 1. INTRODUCTION

A general trend in computers today is to increase the complexity of architectures commensurate with the increasing potential of implementation technologies. Consequences of this complexity are increased design time, more design errors, inconsistent implementations, and the delay of single chip implementation[7]. The Reduced Instruction Set Computer (RISC) Project investigates a VLSI alternative to this trend. Our initial design is called RISC I.

A judicious choice of a small set of the most often used instructions combined with an architecture tailored to efficient execution of this set can yield a machine of surprisingly high throughput. In addition, a single-chip implementation of a simpler machine makes more effective use of limited resources such as the number of transistors, area, and power consumption of present-day VLSI chips[8]. Simplicity of the instruction set leads to a small control section, a comparatively short machine cycle, and a reduced design cycle time.

Students taking part in a multi-term course sequence designed two different NMOS versions of RISC I. The "Gold" group (Fitzpatrick, Foderaro, Peek, Peshkess, and Van Dyke) designed a complete 32-bit microprocessor, currently being fabricated. The "Blue" group (Katevenis and Sherburne) started from the same basic organization but introduced a more sophisticated timing scheme in order to shorten the machine cycle and also reduce chip area. At present, only the data path of this more ambitious design has been completed. The chips were designed using only horizontal and vertical lines ("Manhattan" design), with the simple and scalable Mead-Conway design rules (fabrication:  $\lambda = 2$  microns, no buried contacts).

At the onset of the design of RISC I we defined the following goals and constraints: (a) find a reasonable compromise between high performance for high-level language programs and a simple, single chip implementation; (b) make the size of all instructions equal to one word and execute all instructions in one machine cycle; (c) emphasize register oriented instructions and restrict memory access to the LOAD and STORE instructions. The resulting architecture has 31 instructions in two formats, uses 32-bit addresses, and supports 8-, 16-, and 32-bit data.

The chip area saved by simplicity of the control circuitry was devoted to a very large set of 32-bit registers. This permits the processor to allocate a new

# Reduced Instruction Set Computer Architectures For Vlsi

**R Sandford**



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