Rapid Prototyping of Application Specific Signal Processors

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Rapid Prototyping Of Application Specific Signal Processors:

Rapid Prototyping of Application Specific Signal Processors Mark A. Richards,Anthony J. Gadient,Geoffrey A. Frank,1997-02-28 Rapid Prototyping of Application Specific Signal Processors presents leading edge research that focuses on design methodology infrastructure support and scalable architectures developed by the 150 million dollar DARPA United States Department of Defense RASSP Program The contributions to this edited work include an introductory overview chapter that explains the origin concepts and status of this effort The RASSP Program is a multi year DARPA Tri Service initiative intended to dramatically improve the process by which complex digital systems particularly embedded signal processors are designed manufactured upgraded and supported This program was originally driven by military applications for signal processing The requirements of military applications for real time signal processing are typically more demanding than those of commercial applications but the time gap between technology employed in advanced military prototypes and commercial products is narrowing rapidly The research on methodologies infrastructure and architectures presented in this book is applicable to commercial signal processing systems that are in design now or will be developed before the end of the decade Rapid Prototyping of Application Specific Signal Processors is a valuable reference for developers of embedded digital systems particularly systems engineers for signal processing systems such as digital TV biomedical image processing systems and telecommunications and for military contractors who are developing signal processing systems This book will also be of interest to managers who are charged with responsibility for creating and maintaining environments and infrastructures for developing large embedded digital systems The chief value for managers will be the defining of methods and processes that reduce development time and cost **Rapid Prototyping of Application Specific Signal Processors (RASSP).** ,1993 This document provides for each of the computer aided design CAD tools in the initial baseline RAASP design environment a description of its role in the environment an assessment of strengths and weaknesses and manufacturer s contact information This RASSP initial design environment is summarized in Table 1 which specified the tool name the manufacturer and a short description of each tool The detailed description and assessment of each tool comprises the remainder of this document following the introduction Rapid Prototyping of Application Specific Signal Processors Program ,1992 This report discusses the results of the TI RASSP study efforts to identify a development process consistent with the RASSP program methodology In this study we defined the concept of a library based system design approach with in cycle and out of cycle development of library elements This report discusses this approach and the issues associated with system hardware and software design tools and manufacturing foundry interfaces required to support a library based system development approach The library based development concept is defined and the modularity and partitioning of a domain specific architecture is discussed A description of the library elements supporting a library based system design approach is provided Requirements issues and approaches to signal processing system design analyses and tradeoffs and system

simulation and validation are discussed Data base representation issues frame words and interfaces required to provide a seamless RASSP development environment are identified Reusable software and library element development issues are addressed Hardware CAD issues associated with library element development system analyses simulation and validation are discussed Manufacturing foundry CAD CIM design tool interfaces and test issues are also discussed A summary of the effort and recommendations for implementation are also included **VLSI Digital Signal Processors** Vijay Madisetti,1995 This is the only book that offers a thorough treatment of the following design and application of programmable digital signal processors formal specification and optimization of signal processing architectures and circuits high level synthesis of DSP architectures and datapaths detailed treatment of application specific integrated circuits ASICs scheduling allocation and assignment algorithms for multiple processor DSP systems and hardware software co design issues in DSP VLSI Digital Signal Processors An Introduction to Rapid Prototyping and Design Synthesis provides a cohesive quantitative and clear exposition of the implementation and prototyping of digital signal processing algorithms on programmable signal processors parallel processing systems and application specific ICs Included are both programmable and dedicated digital signal processors and discussions of the latest optimization methods and the use of computer aided design techniques *Special Issue on the Rapid Prototyping of Application Specific Signal Processors (RASSP) Program* ,1997 **Rapid Prototyping of Application Specific Signal Processors (RASSP) Program - Study Phase** ,1992 This is the final report for the Rapid Prototyping of Applications Specific Signal Processors RASSP Program Study Phase This study represents a five month contract effort DARPA contract number MDA972 92 C 0057 performed by Honeywell s Systems and Research Center for the Defense Advanced Research Projects Agency DARPA The Broad objective of this study was to produce information that would aid the Government program manager to manage the risks inherent in the implementation phase of the RASSP program This meant 1 identifying the risks and problem areas that might be encountered during the implementation phase and 2 suggesting risk reducers or solutions that could be used to minimize or solve these problems Ultimately this meant recommending an approach for the implementation phase and also identifying potential areas for further work The RASSP program embraces two tightly coupled focuses one related to process or methodology and the other related to target prototype or product systems These are discussed in detail in this final report **Rapid Prototyping of Application Specific Signal Processors (RASSP), RDE System Description** ,1995 The purpose of this document is to describe the Lockheed Sanders Team KASSP Design Environment RDE The RDE provides a working environment to support users of the RASSP process to develop signal processing systems more quickly and with greater quality than was previously achievable The RDE is a CAD tool independent process management system that supports distributed development This document describes the RDE and the components that make up the environment AN **Application Specific Processors** Earl E. Swartzlander Jr.,2012-12-06 Application Specific Processors is written for use by engineers who are developing specialized

systems application specific systems Traditionally most high performance signal processors have been realized with application specific processors The explanation is that application specific processors can be tailored to exactly match the usually very demanding application requirements The result is that no processing power is wasted for unnecessary capabilities and maximum performance is achieved A disadvantage is that such processors have been expensive to design since each is a unique design that is customized to the specific application In the last decade computer aided design systems have been developed to facilitate the development of application specific integrated circuits The success of such ASIC CAD systems suggests that it should be possible to streamline the process of application specific processor design Application Specific Processors consists of eight chapters which provide a mixture of techniques and examples that relate to application specific processing The inclusion of techniques is expected to suggest additional research and to assist those who are faced with the requirement to implement efficient application specific processors The examples illustrate the application of the concepts and demonstrate the efficiency that can be achieved via application specific processors The chapters were written by members and former members of the application specific processing group at the University of Texas at Austin The first five chapters relate to specific arithmetic which often is the key to achieving high performance in application specific processors The next two chapters focus on signal processing systems and the final chapter examines the interconnection of possibly disparate elements to create systems *Rapid-Prototyping of Application Specific Signal Processors (RASSP) Education and Facilitation* ,2000 The Rapid Prototyping of Application Specific Signal Processors RASSP program was a major DARPA Tri Service initiative to reinvent the process by which embedded digital signal processors were developed The goal of the DARPA Tri service RASSP program was to dramatically improve the design process for complex digital systems particularly embedded signal processors A key objective was to reduce the total product development time by at least a factor of four while making similar improvements in product quality and life cycle cost Also important was the ability to field state of the art equipment at system build time and to rapidly upgrade the system throughout its life cycle The RASSP Education and Facilitation E F program was an unprecedented program set up to disseminate the information developed by 24 other RASSP programs to enable a paradigm shift in the way signal processors were designed The RASSP E F program is made up of four distinct functions education information server interface and transition Major accomplishments include the establishment and maintenance of a web server the publication of the RASSP Digest development of educational and training materials and technology transfer including executive seminars workshops RASSP Course Modules and IEEE publication of two RASSP CD ROMs The second edition of the RASSP CD ROM presents the essence of the knowledge from the entire RASSP program The web server has been relocated but is still operational **Cryptographic Hardware and Embedded Systems** Cetin K. Koc,Christof Paar,2003-07-31 This book constitutes the refereed proceedings of the First International Workshop on Cryptographic Hardware and Embedded Systems CHES 99 held in Worcester MA USA in August 1999 The 27

revised papers presented together with three invited contributions were carefully reviewed and selected from 42 submissions The papers are organized in sections on cryptographic hardware hardware architectures smartcards and embedded systems arithmetic algorithms power attacks true random numbers cryptographic algorithms on FPGAs elliptic curve implementations new cryptographic schemes and modes of operation **Proceedings of the 1995 International Conference on Parallel Processing** Dharma P. Agrawal,1995-08-08 This set of technical books contains all the information presented at the 1995 International Conference on Parallel Processing This conference held August 14 18 featured over 100 lectures from more than 300 contributors and included three panel sessions and three keynote addresses The international authorship includes experts from around the globe from Texas to Tokyo from Leiden to London Compiled by faculty at the University of Illinois and sponsored by Penn State University these Proceedings are a comprehensive look at all that s new in the field of parallel processing *Cryptographic Hardware and Embedded Systems* Çetin K. Koç,Christof Paar,1999 This book constitutes the refereed proceedings of the First International Workshop on Cryptographic Hardware and Embedded Systems CHES 99 held in Worcester MA USA in August 1999 The 27 revised papers presented together with three invited contributions were carefully reviewed and selected from 42 submissions The papers are organized in sections on cryptographic hardware hardware architectures smartcards and embedded systems arithmetic algorithms power attacks true random numbers cryptographic algorithms on FPGAs elliptic curve implementations new cryptographic schemes and modes of operation **Distributed and Parallel Embedded Systems** Franz J. Rammig,2013-03-09 Embedded systems are becoming one of the major driving forces in computer science Furthermore it is the impact of embedded information technology that dictates the pace in most engineering domains Nearly all technical products above a certain level of complexity are not only controlled but increasingly even dominated by their embedded computer systems Traditionally such embedded control systems have been implemented in a monolithic centralized way Recently distributed solutions are gaining increasing importance In this approach the control task is carried out by a number of controllers distributed over the entire system and connected by some interconnect network like fieldbuses Such a distributed embedded system may consist of a few controllers up to several hundred as in today s top range automobiles Distribution and parallelism in embedded systems design increase the engineering challenges and require new development methods and tools This book is the result of the International Workshop on Distributed and Parallel Embedded Systems DIPES 98 organized by the International Federation for Information Processing IFIP Working Groups 10 3 Concurrent Systems and 10 5 Design and Engineering of Electronic Systems The workshop took place in October 1998 in Schloss Eringerfeld near Paderborn Germany and the resulting book reflects the most recent points of view of experts from Brazil Finland France Germany Italy Portugal and the USA The book is organized in six chapters Formalisms for Embedded System Design IP based system design and various approaches to multi language formalisms Synthesis from Synchronous Asynchronous Specification Synthesis techniques based on Message

Sequence Charts MSC StateCharts and Predicate Transition Nets Partitioning and Load Balancing Application in simulation models and target systems Verification and Validation Formal techniques for precise verification and more pragmatic approaches to validation Design Environments for distributed embedded systems and their impact on the industrial state of the art Object Oriented Approaches Impact of OO techniques on distributed embedded systems LIST This volume will be essential reading for computer science researchers and application developers **Specification and Design Methodology for Real-Time Embedded Systems** Randall S. Janka,2012-12-06 Specification and design methodology has seen significant growth as a research area over the last decade tracking but lagging behind VLSI design technology in general and the CAD industry in particular The commercial rush to market tries to leverage existing technology which fuels CAD design tool development Paralleling this is very active basic and applied research to investigate and move forward rational and effective methodologies for accomplishing digital design especially in the field of hardware software codesign It is this close relationship between industry and academia that makes close cooperation between researchers and practitioners so important and monographs like this that combine both abstract concept and pragmatic implementation deftly bridge this often gaping chasm It was at the IEEE ACM Eighth International Symposium on Hardware Software Codesign where I met the author of this monograph Dr Randall Janka who was presenting some of his recent dissertation research results on specification and design methodology or as he has so succinctly defined this sometimes ambiguous concept the tools and rules Where so many codesign researchers are trying to prove out different aspects of codesign and using toy applications to do so Dr Janka had developed a complete specification and design methodology and prototyped the infrastructure and proven its viability utility and effectiveness using a demanding real world application of a real time synthetic aperture radar imaging processor that was implemented with embedded parallel processors **ESL Design and Verification** Grant Martin,Brian Bailey,Andrew Piziali,2010-07-27 Visit the authors companion site http www electronicsystemlevel com Includes interactive forum with the authors Electronic System Level ESL design has mainstreamed it is now an established approach at most of the world s leading system on chip SoC design companies and is being used increasingly in system design From its genesis as an algorithm modeling methodology with no links to implementation ESL is evolving into a set of complementary methodologies that enable embedded system design verification and debug through to the hardware and software implementation of custom SoC system on FPGA system on board and entire multi board systems This book arises from experience the authors have gained from years of work as industry practitioners in the Electronic System Level design area they have seen SLD or ESL go through many stages and false starts and have observed that the shift in design methodologies to ESL is finally occurring This is partly because of ESL technologies themselves are stabilizing on a useful set of languages being standardized SystemC is the most notable and use models are being identified that are beginning to get real adoption ESL DESIGN VERIFICATION offers a true prescriptive guide to ESL that reviews its past and outlines the best practices of

today Table of ContentsCHAPTER 1 WHAT IS ESL CHAPTER 2 TAXONOMY AND DEFINITIONS FOR THE ELECTRONIC SYSTEM LEVEL CHAPTER 3 EVOLUTION OF ESL DEVELOPMENT CHAPTER 4 WHAT ARE THE ENABLERS OF ESL CHAPTER 5 ESL FLOW CHAPTER 6 SPECIFICATIONS AND MODELING CHAPTER 7 PRE PARTITIONING ANALYSIS CHAPTER 8 PARTITIONING CHAPTER 9 POST PARTITIONING ANALYSIS AND DEBUG CHAPTER 10 POST PARTITIONING VERIFICATION CHAPTER 11 HARDWARE IMPLEMENTATION CHAPTER 12 SOFTWARE IMPLEMENTATION CHAPTER 13 USE OF ESL FOR IMPLEMENTATION VERIFICATION CHAPTER 14 RESEARCH EMERGING AND FUTURE PROSPECTS APPENDIX LIST OF ACRONYMS Provides broad comprehensive coverage not available in any other such book Massive global appeal with an internationally recognised author team Crammed full of state of the art content from notable industry experts   Application Specific Processors Earl E. Swartzlander,1997 Application Specific Processors consists of eight chapters which provide a mixture of techniques and examples that relate to application specific processing The inclusion of techniques is expected to suggest additional research and to assist those who are faced with the requirement to implement efficient application specific processors The examples illustrate the application of the concepts and demonstrate the efficiency that can be achieved via application specific processors The chapters were written by members and former members of the application specific processing group at the University of Texas at Austin   **Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology** ,1997   **Proceedings** ,1994   *The Fifth International Workshop on Rapid System Prototyping* Nick Kanopoulos,1994 Proceedings of the June 1994 workshop presenting 25 papers on models for system simulation emulation in a hierarchical sense software to hardware mapping software prototyping and validation prototyping environments of hardware simulators and experiences from specific system prototyping projects Lacks an index Annotation copyright by Book News Inc Portland OR   **IEEE/CPMT International Electronics Manufacturing Technology Symposium** ,1994

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