

# Coupled device, circuit and interconnect simulation

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## Abstract:

*In this paper, we discuss several aspects that are related to coupling device, circuit and interconnect simulation software. Straightforward co-simulation is too time-consuming, and hence reduced order modelling must be used in order to summarize the behaviour of individual simulations into compact models. From a theoretical point of view, the problem is complicated by the fact that equations of different type are being coupled. Mathematical techniques are indispensable for guaranteeing acceptable simulation times.*

*The European project CODESTAR aims at providing a framework in which the aforementioned coupled simulations can be performed. The examples given in this paper have been taken from that project.*

## 1. Introduction

For the design of complex integrated systems, knowledge of the electromagnetic coupling in passive components like inductors, capacitors and critical parts of net lists are indispensable. Today's extraction software tools use the static approach to quantify this coupling, thereby ignoring the Maxwell or wave-dynamic aspect of electromagnetic radiation. Whereas such an approach is valid at moderate frequencies, high-frequency effects are a major design concern for the next generation of architectures. The International Technology Roadmap for Semiconductors recognizes the lack of appropriate future design tools. In particular design tools that include high frequency effects are a difficult challenge for a successful implementation of the 65 nm node corresponding to circuit frequencies exceeding 5 GHz. The effects are physically understood, but TCAD software programs that can deal with them are not available. Figure 1 (inspired by [6]) summarizes the effects that play a role in the analysis of passive structures: electric and magnetic coupling of segments through air and oxide, current crowding at edges due to the skin effect and eddy currents, proximity effects due to presence of nearby segments, radiation, substrate injection, and substrate current caused by ohmic, eddy and displacement currents.

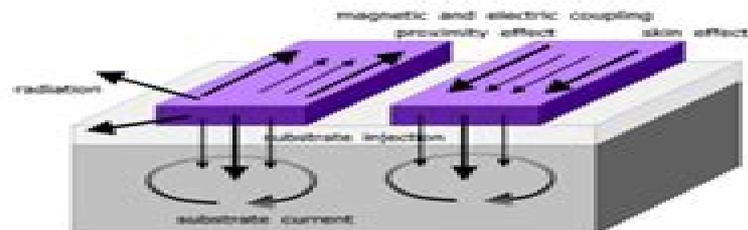


Figure 1. Summary of effects occurring in passive structures.

To accelerate the design of high-frequency passive on-chip structures and interconnects, the development of new modelling algorithms is needed. This task is addressed in the CODESTAR project. The resulting software will be used in a design cycle, starting from standardized geometrical data (GDS II format), and returning as output a manageable simulation net list that can be coupled to a network simulator such as SPICE or Pstar.

The situation becomes even more complicated when substrate noise analysis is required. As feature sizes decrease, substrate coupling noise may cause design failures and poor yields due to injected currents disturbing the operation of sensitive components. Any design targeted at sub-quarter micron process technologies may be vulnerable to substrate parasitics. Rule of thumb methodologies may turn out to be inadequate or lead to over-engineered designs. Reliable results can only be obtained by taking into account semiconductor physics. Tools like SubstrateStorm from Cadence perform such analyses by supplying RC net lists and reduced RC net lists, which can be coupled to network simulators. More accurate results are obtained when drift-diffusion models of semiconductor devices are used. In section 3 an example is given discussing precisely this topic, showing that it is indeed possible to couple device, circuit and interconnect simulations to obtain reliable models for substrate coupling noise.

# Principles Of Circuit And Interconnect Simulation

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## **Principles Of Circuit And Interconnect Simulation:**

**Circuit Simulation Principles and Techniques and Their Application Toward Interconnect Simulation** Kirk Alan Ingemunson,1994     **Coupled Multiscale Simulation and Optimization in Nanoelectronics** Michael Günther,2015-06-15

Designing complex integrated circuits relies heavily on mathematical methods and calls for suitable simulation and optimization tools The current design approach involves simulations and optimizations in different physical domains device circuit thermal electromagnetic and in a range of electrical engineering disciplines logic timing power crosstalk signal integrity system functionality COMSON was a Marie Curie Research Training Network created to meet these new scientific and training challenges by a developing new descriptive models that take these mutual dependencies into account b combining these models with existing circuit descriptions in new simulation strategies and c developing new optimization techniques that will accommodate new designs The book presents the main project results in the fields of PDAE modeling and simulation model order reduction techniques and optimization based on merging the know how of three major European semiconductor companies with the combined expertise of university groups specialized in developing suitable mathematical models numerical schemes and e learning facilities In addition a common Demonstrator Platform for testing mathematical methods and approaches was created to assess whether they are capable of addressing the industry s problems and to educate young researchers by providing hands on experience with state of the art problems     [Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS Nodes](#) Hsiao-Hsuan Liu,Francky Catthoor,2024-12-20

Modern computing engines CPUs GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro

level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes

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### **Table of Contents Principles Of Circuit And Interconnect Simulation**

1. Understanding the eBook Principles Of Circuit And Interconnect Simulation
  - The Rise of Digital Reading Principles Of Circuit And Interconnect Simulation
  - Advantages of eBooks Over Traditional Books
2. Identifying Principles Of Circuit And Interconnect Simulation
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in an Principles Of Circuit And Interconnect Simulation
  - User-Friendly Interface
4. Exploring eBook Recommendations from Principles Of Circuit And Interconnect Simulation
  - Personalized Recommendations
  - Principles Of Circuit And Interconnect Simulation User Reviews and Ratings
  - Principles Of Circuit And Interconnect Simulation and Bestseller Lists

5. Accessing Principles Of Circuit And Interconnect Simulation Free and Paid eBooks
  - Principles Of Circuit And Interconnect Simulation Public Domain eBooks
  - Principles Of Circuit And Interconnect Simulation eBook Subscription Services
  - Principles Of Circuit And Interconnect Simulation Budget-Friendly Options
6. Navigating Principles Of Circuit And Interconnect Simulation eBook Formats
  - ePub, PDF, MOBI, and More
  - Principles Of Circuit And Interconnect Simulation Compatibility with Devices
  - Principles Of Circuit And Interconnect Simulation Enhanced eBook Features
7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of Principles Of Circuit And Interconnect Simulation
  - Highlighting and Note-Taking Principles Of Circuit And Interconnect Simulation
  - Interactive Elements Principles Of Circuit And Interconnect Simulation
8. Staying Engaged with Principles Of Circuit And Interconnect Simulation
  - Joining Online Reading Communities
  - Participating in Virtual Book Clubs
  - Following Authors and Publishers Principles Of Circuit And Interconnect Simulation
9. Balancing eBooks and Physical Books Principles Of Circuit And Interconnect Simulation
  - Benefits of a Digital Library
  - Creating a Diverse Reading Collection Principles Of Circuit And Interconnect Simulation
10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
11. Cultivating a Reading Routine Principles Of Circuit And Interconnect Simulation
  - Setting Reading Goals Principles Of Circuit And Interconnect Simulation
  - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Principles Of Circuit And Interconnect Simulation
  - Fact-Checking eBook Content of Principles Of Circuit And Interconnect Simulation
  - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
14. Embracing eBook Trends
- Integration of Multimedia Elements
  - Interactive and Gamified eBooks

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