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Bit Sliced Parallel
Computer (USA)

Rushton, A.

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Reconfigurable Processor Array A Bit Sliced Parallel Computer (Usa) A. Rushton,1991-02 *Principles of Auditing/Study Guide* Walter B. Meigs,E. Larsen,R. Meigs,1988-12-01 Reconfigurable Processor-array Andrew Rushton,1989 This book investigates enhancements to the conventional bit serial PE with the aim of improving its performance in situations where the small grain parallelism of a single instruction stream multiple data stream SIMD class parallel computer architecture is inefficient

Forthcoming Books Rose Army,1989-05 *Publishers Trade List Annual, 1992, 1992 Paperbound Books in Print* ,1991 *The Publishers' Trade List Annual* ,1992 **Whitaker's Book List** ,1989 *The British National Bibliography* Arthur James Wells,1968 *Whitaker's Books in Print* ,1998 **Index to IEEE Publications** Institute of Electrical and Electronics Engineers,1987 Issues for 1973 cover the entire IEEE technical literature

Data Parallel C on a Reconfigurable Logic Array Maya B. Gokhale,Brian Schott,Institute for Defense Analyses,1994 Abstract The existence of reconfigurable logic arrays has made it possible to create on the same physical hardware platform many different virtual circuits a configuration bit stream loaded into the logic array determines the virtual circuit which is to be emulated The virtual logic can be used to create new instructions which supplement the instruction set of a conventional processor as demonstrated for example in 2 and 3 or alternatively can operate as a parallel co processor as shown in the Splash systems 8 and 9 The ease of hardware reconfiguration has not been accompanied by a corresponding capability in the software environment In most cases schematic capture tools textual hardware description languages or low level vendor specific tools must be used to create new configurations Research into high level synthesis for reconfigurable arrays has begun however as evidenced by the PRISM 2 tools of 3 and the dbC translation system of 9 The ability to write algorithms for these arrays in high level procedural language is key to their effective use In this paper we describe the data parallel bit C system which is used to program a reconfigurable logic array as a custom SIMD co processor The dbC language has bit oriented extensions to C which give the programmer control over the size of parallel data objects so that the data size requirements of the algorithm can be accurately reflected in the hardware The data parallel extensions provide the ability to define a SIMD processor array to operate on data in the processors memories to perform global reductions over the processor array and to communicate data between nearest neighbor processing elements We describe the major components of our translation system and show how it is mapped onto the Splash 2 system

Reconfigurable Processor Array A. Rushton,E Jerome McCarthy,1991-02

Reconfigurable Massively Parallel Computers Hungwen Li,Quentin F. Stout,1991 Offers guidance on three areas of the complex world of reconfigurable massively parallel computers architecture mapping algorithms to the architecture and fault tolerance The material is addressed to students and professionals interested in the exploitation of array processing

Design of a Bit-sliced Processor Array with Built-in-self-test Paul Chunhei Mui,1984 The overall objective of this report is to present an integrated approach to the design of bit sliced processor arrays with built in self test

The conventional approach of making each bit sliced processor chip self testing is not used Rather a new approach of using an extra chip to test a processor array fo any size and itself is used The classical stuck at fault model is not suitable for VLSI circuits Rather a functional level fault model is used Ech module of the processor array is tested exhaustively The test responses of a fault free processor array are made identical so that they can be easily monitored with no loss in fault coverage The tester chip tests itself while it is testing the processor array The fault coverages for both the tester chip and the processor array are high the performance degradation is minimal the area overhead is low especially for large processor arrays and the test length is short so tests can be performed more frequently A VLSI design of the tester chip has been done with a 2 microns NMOS process Author **An Investigation of a Parallel Reconfigurable Processor** Stanford University. Stanford Electronics Laboratories,Joost Mortelmans,1974 *Reconfigurable Computing* Maya B. Gokhale,Paul S. Graham,2006-07-04 A one of a kind survey of the field of Reconfigurable Computing Gives a comprehensive introduction to a discipline that offers a 10X 100X acceleration of algorithms over microprocessors Discusses the impact of reconfigurable hardware on a wide range of applications signal and image processing network security bioinformatics and supercomputing Includes the history of the field as well as recent advances Includes an extensive bibliography of primary sources [A Computer Architecture Based on Reconfigurable Co-processor Modules](#) Mehmet Can Ertem,1986 [Invasive Tightly Coupled Processor Arrays](#) VAHID LARI,2016-07-19 This book introduces new massively parallel computer MPSoC architectures called invasive tightly coupled processor arrays It proposes strategies architecture designs and programming interfaces for invasive TCPAs that allow invading and subsequently executing loop programs with strict requirements or guarantees of non functional execution qualities such as performance power consumption and reliability For the first time such a configurable processor array architecture consisting of locally interconnected VLIW processing elements can be claimed by programs either in full or in part using the principle of invasive computing Invasive TCPAs provide unprecedented energy efficiency for the parallel execution of nested loop programs by avoiding any global memory access such as GPUs and may even support loops with complex dependencies such as loop carried dependencies that are not amenable to parallel execution on GPUs For this purpose the book proposes different invasion strategies for claiming a desired number of processing elements PEs or region within a TCPA exclusively for an application according to performance requirements It not only presents models for implementing invasion strategies in hardware but also proposes two distinct design flavors for dedicated hardware components to support invasion control on TCPAs **Reconfigurable Parallel Architectures for Special Purpose Computing** Moore School of Electrical Engineering. Department of Computer and Information Science,R. Krishnamurti,1987

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