

eight lines. Therefore, for the simple three-state driver shown in Figure 7-2, 24 for data input and 24 for data output to each device might have dozens of memory devices and 100 pins for interconnecting lines.

A solution to this interconnection problem is the use of a bus, as shown in Figure 7-2. Note how much simpler the interconnection is. A single line is used to interconnect all the devices, and the wires of a single line traveling into or out of the processor. This positive characteristic, with little increase in interconnection complexity, a computer technique is that, since all devices share the same data bus, the processor data at any given time. The address and control lines (data processor) provide the necessary control to send a message.



Figure 7-2 Data Exchange Using a Bus to Reduce the Number of Interconnecting Lines

THE THREE-STATE BUS

The three-state driver makes the shared data bus possible. In simplicity, a single-line bus is discussed first, however, the same principle applies to a multi-line bus. (The same principle applies to a multi-line bus.)

The three-state bus is like a telephone call line. There are many talkers connected to it. Figure 7-3 shows two talkers (three-state drivers) and two listeners (three-state drivers) connected to a bus line.

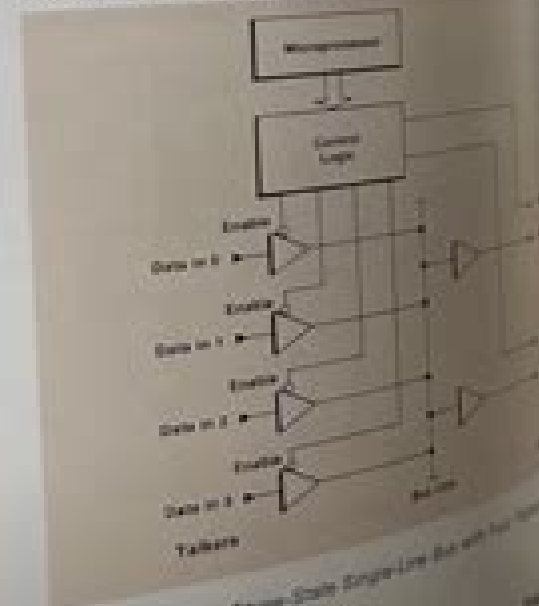


Figure 7-3 Three-State Single-Line Bus with Two Talkers

more than one driver (talker) to be active at any given time, if more than one driver is enabled, the data on the bus would be meaningless. When a driver is enabled, the data on the bus is placed on the bus. All of the other drivers are disabled, their outputs are in a high-impedance (floating) state, so they have no effect on the logic state of the bus. (For an explanation of the symbolology used in this course, refer to Appendix D.)

There can be many listeners on the bus. Since all they do is listen, more than one listener can be enabled at the same time. In general, however, the data on the bus is intended for one of them in particular. The control logic generates signals (data enable) to tell selected listeners that the data on the bus is intended for them. A data enable can be used, for example, to clock the data from the bus into a flip-flop. The inputs to the control logic are the address and control buses coming from the microprocessor. (See Figure 7-4.)

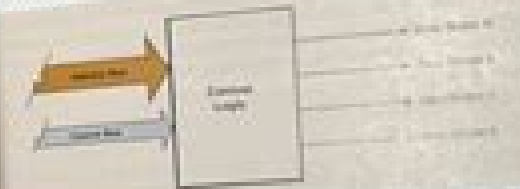


Figure 7-4 Control Logic Selects Device to be Receiver of Data Transfer

The devices just described are unidirectional. They will either output to listeners, but not listen. Bidirectional devices also exist, which are both writers and readers. Figure 7-5 shows a bus with two talker-listeners. For the sake of simplicity, only two have been shown, but there could be many more. Each talker-listener is provided with two control signals: the output enable signal for the three-state driver and the data enable for the input. An example of a bidirectional device is a RAM, which can read and write data.

As an example of how this process works, suppose device A in Figure 7-5 must send a piece of data to device B. The control logic will output enable A true

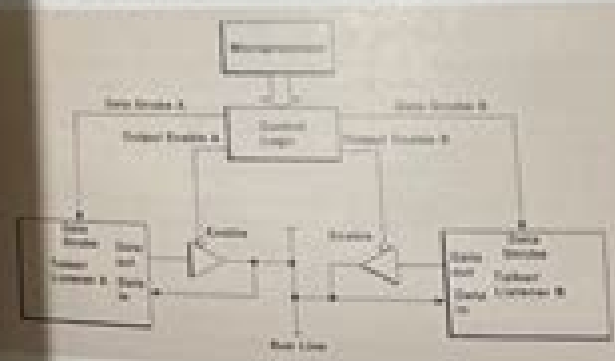


Figure 7-5 Bidirectional Talker-Listeners Connected to Bus Line

Labels of Bidirectional Microprocessors

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