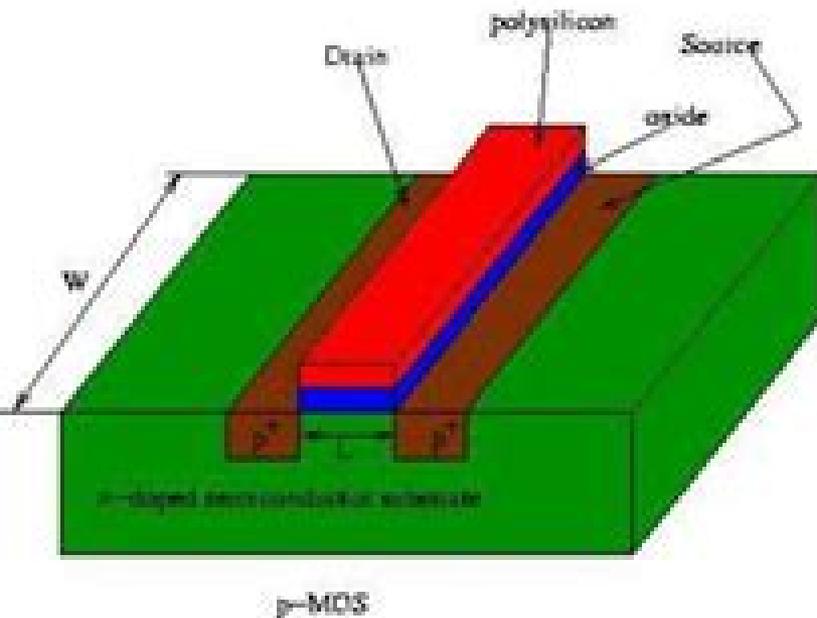


# Structure and Operation of MOS Transistor



- The two p<sup>+</sup> regions will be current-conducting terminals of this device.
- A conducting channel is eventually formed through applied gate voltage in the section between the drain and the source diffusion regions.
- The channel Length and Width are very important parameters which can be used to control some of the electrical properties of the MOSFET.

# Operation And Modeling Of The Mos Transistor

**J Ma**



## **Operation And Modeling Of The Mos Transistor:**

*Operation and Modeling of the MOS Transistor* Yannis Tsividis, Colin McAndrew, 2011 The MOS Metal Oxide Semiconductor transistor is the most important building block of modern silicon integrated circuits This book fills an important gap in the literature by presenting a unified treatment of the operation and modeling of the MOS transistor that is complemented with extensive intuitive discussions The MOS transistor is the dominant VLSI Very Large Scale Integration device and understanding of this device is mandatory for those people planning a career in device physics and modeling as well as in circuit design Especially important for university courses there is a logical systematic and progressive description that starts with semiconductor fundamentals and builds up to a comprehensive understanding of the basics of MOS transistors For practicing professionals there are details of nuances observed in MOS transistor behavior and various approaches to modeling these are presented Detailed derivations are given for modeling dc currents charges for large signal operation small signal operation at low frequencies and high frequencies and noise

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each transistor High performance analog circuit design requires a very detailed model of the transistor describing accurately its static and dynamic behaviors its noise and matching limitations and its temperature variations The charge based EKV Enz Krummenacher Vittoz MOS transistor model for IC design has been developed to provide a clear understanding of the device properties without the use of complicated equations All the static dynamic noise non quasi static models are completely described in terms of the inversion charge at the source and at the drain taking advantage of the symmetry of the device Thanks to its hierarchical structure the model offers several coherent description levels from basic hand calculation equations to complete computer simulation model It is also compact with a minimum number of process dependant device parameters Written by its developers this book provides a comprehensive treatment of the EKV charge based model of the MOS transistor for the design and simulation of low power analog and RF ICs Clearly split into three parts the authors systematically examine the basic long channel intrinsic charge based model including all the fundamental aspects of the EKV MOST model such as the basic large signal static model the noise model and a discussion of temperature effects and matching properties the extended charge based model presenting important information for understanding the operation of deep submicron devices the high frequency model setting out a complete MOS transistor model required for designing RF CMOS integrated circuits Practising engineers and circuit designers in the semiconductor device and electronics systems industry will find this book a valuable guide to the modelling of MOS transistors for integrated circuits It is also a useful reference for advanced students in electrical and computer engineering

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*Process and Device Modeling for Microelectronics* Giorgio Baccarani,1993 The 11 invited papers in this volume written by experts in the field report on current trends and significant research findings in the modeling and simulation of semiconductor devices and processes monitoring the rapid scientific growth that has occurred in this area The project Materials and Devices for Solid State Electronics MADESS funded by Italy s National Research Council started in 1987 and

lasted 5 years The project addressed five main research areas VLSI Technology and Device Physics Microwave and Optoelectronic Devices Sensors Semiconductor Power Devices and Reliability and Diagnostics Encompassing a large spectrum of activities ranging from material science to system architecture research units included universities public research laboratories and industry The amount of resources made available by the project to the scientific community in the above areas has turned out to be a major impetus for growth in this scientific field In addition it has enhanced various forms of cooperation between research and industry contributing to the development of a new consciousness concerning the role of microelectronics in modern society The contributions in this volume are of worldwide interest and will help to stimulate future research and analysis in this field

Floating Gate Devices: Operation and Compact Modeling Paolo Pavan, Luca Larcher, Andrea Marmiroli, 2007-05-08 Floating Gate Devices Operation and Compact Modeling focuses on standard operations and compact modeling of memory devices based on Floating Gate architecture Floating Gate devices are the building blocks of Flash EPROM EEPROM memories Flash memories which are the most versatile nonvolatile memories are widely used to store code BIOS Communication protocol Identification code and data solid state Hard Disks Flash cards for digital cameras The reader who deals with Floating Gate memory devices at different levels from test structures to complex circuit design will find an essential explanation on device physics and technology and also circuit issues which must be fully understood while developing a new device Device engineers will use this book to find simplified models to design new process steps or new architectures Circuit designers will find the basic theory to understand the use of compact models to validate circuits against process variations and to evaluate the impact of parameter variations on circuit performances Floating Gate Devices Operation and Compact Modeling is meant to be a basic tool for designing the next generation of memory devices based on FG technologies

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