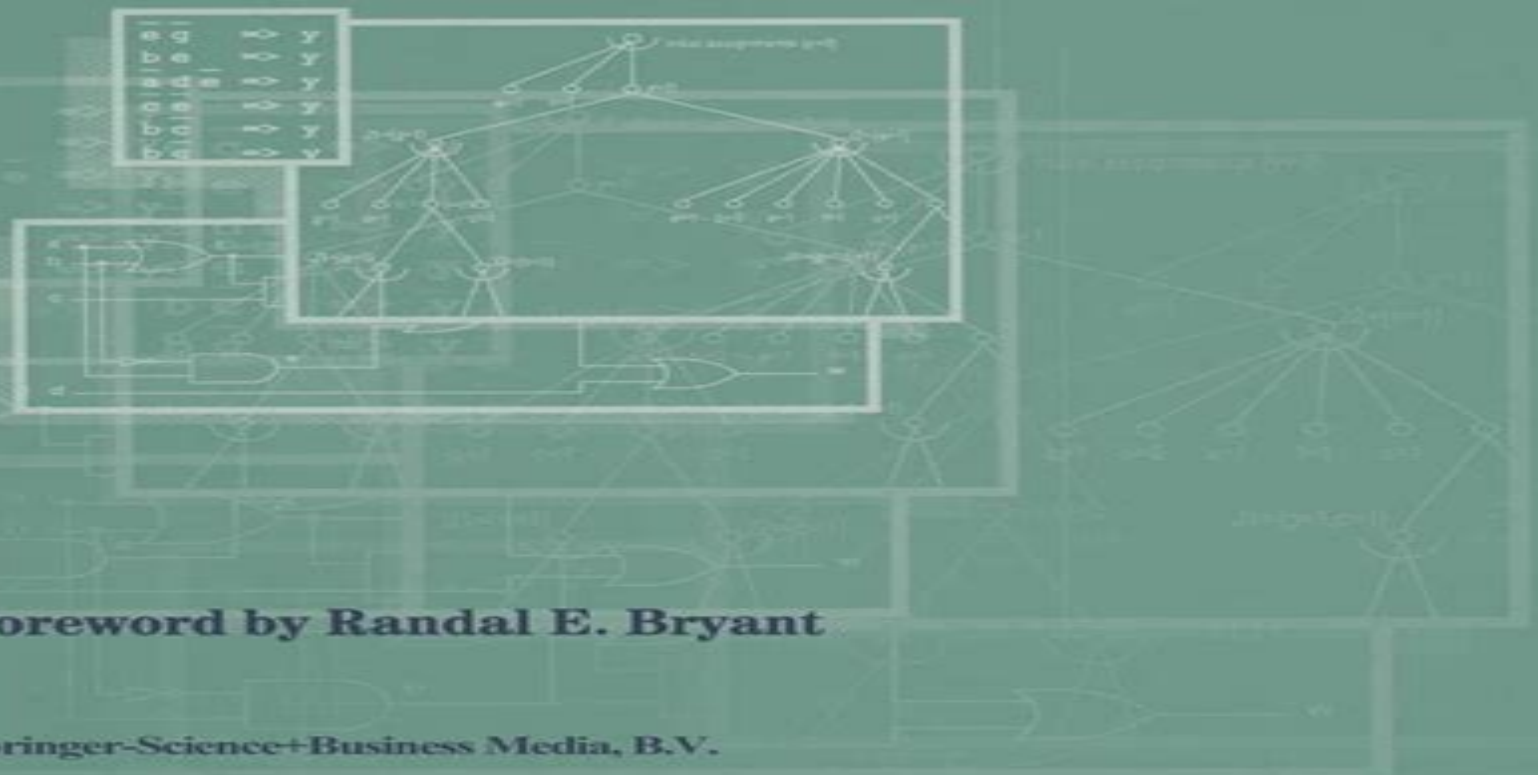


Wolfgang Kunz and Dominik Stoffel

# Reasoning in Boolean Networks

Logic Synthesis and  
Verification Using Testing Techniques



Foreword by Randal E. Bryant

Springer-Science+Business Media, B.V.

# Reasoning In Boolean Networks Logic Synthesis And Verification Using Testing Techniques

**Siddappa N.Byrareddy**



## **Reasoning In Boolean Networks Logic Synthesis And Verification Using Testing Techniques:**

**Reasoning in Boolean Networks** Wolfgang Kunz, Dominik Stoffel, 2013-03-09 Reasoning in Boolean Networks provides a detailed treatment of recent research advances in algorithmic techniques for logic synthesis test generation and formal verification of digital circuits The book presents the central idea of approaching design automation problems for logic level circuits by specific Boolean reasoning techniques While Boolean reasoning techniques have been a central element of two level circuit theory for many decades Reasoning in Boolean Networks describes a basic reasoning methodology for multi level circuits This leads to a unified view on two level and multi level logic synthesis The presented reasoning techniques are applied to various CAD problems to demonstrate their usefulness for today s industrially relevant problems Reasoning in Boolean Networks provides lucid descriptions of basic algorithmic concepts in automatic test pattern generation logic synthesis and verification and elaborates their intimate relationship to provide further intuition and insight into the subject Numerous examples are provide for ease in understanding the material Reasoning in Boolean Networks is intended for researchers in logic synthesis VLSI testing and formal verification as well as for integrated circuit designers who want to enhance their understanding of basic CAD methodologies [Delay Fault Testing for VLSI Circuits](#) Angela Krstic, Kwang-Ting (Tim) Cheng, 2012-12-06 In the early days of digital design we were concerned with the logical correctness of circuits We knew that if we slowed down the clock signal sufficiently the circuit would function correctly With improvements in the semiconductor process technology our expectations on speed have soared A frequently asked question in the last decade has been how fast can the clock run This puts significant demands on timing analysis and delay testing Fueled by the above events a tremendous growth has occurred in the research on delay testing Recent work includes fault models algorithms for test generation and fault simulation and methods for design and synthesis for testability The authors of this book Angela Krstic and Tim Cheng have personally contributed to this research Now they do an even greater service to the profession by collecting the work of a large number of researchers In addition to expounding such a great deal of information they have delivered it with utmost clarity To further the reader s understanding many key concepts are illustrated by simple examples The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice In that sense this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems Tech niques for path delay testing and for use of slower test equipment to test high speed circuits are of particular interest

**Theory and Applications of Satisfiability Testing - SAT 2008** Hans Kleine Büning, Xishun Zhao, 2008-05-07 This volume contains the papers presented at the 11th International Conference on Theory and Applications of Satisfiability Testing SAT 2008 The series of International Conferences on Theory and Applications of Satisfiability Testing SAT has evolved from a first workshop on SAT in 1996 to an annual international conference which is a platform for researchers studying various aspects of the propositional satisfiability problem and its applications In the past the SAT conference venue alternated

between Europe and North America For the first time the conference venue was in Asia more precisely at the Zhudao Guest House near Sun Yat Sen University in Guangzhou P R China Many hard combinatorial problems can be encoded into SAT Therefore improvements on heuristics on the practical side as well as theoretical insights into SAT apply to a large range of real world problems More specifically many important practical verification problems can be rephrased as SAT problems This applies to verification problems in hardware and software Thus SAT is becoming one of the most important core technologies to verify secure and dependable systems The topics of the conference span practical and theoretical research on SAT and its applications and include but are not limited to proof systems proof complexity search algorithms heuristics analysis of algorithms hard instances randomized formulae problem encodings industrial applications solvers splitters tools case studies and empirical results SAT is interpreted in a rather broad sense besides propositional satisfiability it includes for example the main of quantified Boolean formulae QBF and satisfiability modulo theories SMT

**Test Resource Partitioning for System-on-a-Chip** Krishnendu Chakrabarty, Vikram Iyengar, Anshuman Chandra, 2002-06-30 Test Resource Partitioning for System on a Chip is about test resource partitioning and optimization techniques for plug and play system on a chip SOC test automation Plug and play refers to the paradigm in which core to core interfaces as well as core to SOC logic interfaces are standardized such that cores can be easily plugged into virtual sockets on the SOC design and core tests can be plugged into the SOC during test without substantial effort on the part of the system integrator The goal of the book is to position test resource partitioning in the context of SOC test automation as well as to generate interest and motivate research on this important topic SOC integrated circuits composed of embedded cores are now commonplace Nevertheless There remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and test challenges are a major contributor to the widening gap between design capability and manufacturing capacity Testing SOCs is especially challenging in the absence of standardized test structures test automation tools and test protocols Test Resource Partitioning for System on a Chip responds to a pressing need for a structured methodology for SOC test automation It presents new techniques for the partitioning and optimization of the three major SOC test resources test hardware testing time and test data volume Test Resource Partitioning for System on a Chip paves the way for a powerful integrated framework to automate the test flow for a large number of cores in an SOC in a plug and play fashion The framework presented allows the system integrator to reduce test cost and meet short time to market requirements

**Formal Equivalence Checking and Design Debugging** Shi-Yu Huang, Kwang-Ting (Tim) Cheng, 2012-12-06 Formal Equivalence Checking and Design Debugging covers two major topics in design verification logic equivalence checking and design debugging The first part of the book reviews the design problems that require logic equivalence checking and describes the underlying technologies that are used to solve them Some novel approaches to the problems of verifying design revisions after intensive sequential transformations such as retiming are described in detail The second part of the book

gives a thorough survey of previous and recent literature on design error diagnosis and design error correction This part also provides an in depth analysis of the algorithms used in two logic debugging software programs ErrorTracer and AutoFix developed by the authors From the Foreword With the adoption of the static sign off approach to verifying circuit implementations the application specific integrated circuit ASIC industry will experience the first radical methodological revolution since the adoption of logic synthesis Equivalence checking is one of the two critical elements of this methodological revolution This book is timely for either the designer seeking to better understand the mechanics of equivalence checking or for the CAD researcher who wishes to investigate well motivated research problems such as equivalence checking of retimed designs or error diagnosis in sequential circuits Kurt Keutzer University of California Berkeley

**Test and Diagnosis for Small-Delay Defects** Mohammad Tehranipoor, Ke Peng, Krishnendu Chakrabarty, 2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations crosstalk and power supply noise Digest of Technical Papers ,2001

**Tutorial Guide** ,2003 *Proceedings* Asim Smailagic, Robert W. Brodersen, 2002 This text contains information on the design and testing of computer hardware presented at the 2002 IEEE Computer Society Annual Symposium on VLSI

*The British National Bibliography* Arthur James Wells, 2003 Proceedings ,2001 XII Symposium on Integrated Circuits and Systems Design Sociedade Brasileira de Computação, IFIP WG 10.5, 1999 Topics in these conference papers include microprocessors design modelling co design analog design high level synthesis digital design synthesis and reconfiguration CAD tools and IP cores

**American Book Publishing Record** ,1997-09 Whitaker's Books in Print ,1998

**Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference 1997, January 28-31, 1997, Makuhari Messe, Nippon Convention Center, Chiba, Japan** IEEE Circuits and Systems Society, 1996 The Asia and South Pacific conference on design automation is the second in a series of biennial international conferences It aims to provide the CAD DA community with the opportunity to present ideas and concepts on upstream design as well as methodologies of downstream design

**IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences** ,1992 *Science Abstracts* ,1995 *Forthcoming Books* Rose Army, 1997

*The Engineering Index Annual* ,1992 Since its creation in 1884 Engineering Index has covered virtually every major engineering innovation from around the world It serves as the historical record of virtually every major engineering innovation of the 20th century Recent content is a vital resource for current awareness new production information technological forecasting and competitive intelligence The world's most comprehensive interdisciplinary engineering database Engineering Index contains over 10.7 million records Each year over 500,000 new abstracts are added from over 5

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